REMARKS

Claims 1-14, 16 and 17 are pending in the present application. Replacement claims 1-14, 16 and 17 have been presented herewith. Claims 15 and 18 have been canceled. Applicants respectfully reserve the right to file a divisional application including claim 18 of the non-elected invention.

Priority Under 35 U.S.C. 119

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

The drawings have been objected to for the reasons stated on page 2 of the current Office Action dated January 14, 2002. The drawings have been corrected in a separate Drawing Correction Approval Request filed concurrently herewith. Fig. 23 has been denoted as "PRIOR ART" as requested by the Examiner. In Fig. 1, reference numeral 118a has been deleted and in Fig. 10 reference numerals 412a and 414a have been added, as requested by the Examiner. The drawings have been further variously corrected as noted in the Drawing Correction Approval Request. Applicants respectfully submit that the drawings are in compliance with 37 C.F.R. §1.84(p)(5), and therefore respectfully urge the Examiner to withdraw the corresponding objections. Corrected formal drawings will prepared and filed upon approval by the Examiner and subsequent

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indication of allowance of the present application.

Specification

The Examiner has required a new title. Accordingly, the title has been amended as "SEMICONDUCTOR DEVICE HAVING A THICK OXIDE LAYER UNDER GATE SIDE WALLS AND METHOD FOR MANUFACTURING THE SAME", to be more clearly indicative of the claims. The Examiner is respectfully requested to approve the amended title.

The disclosure has been objected to because of the typographical errors as noted on page 3 of the Office Action. The specification and claims have been variously amended in view of this objection. The Examiner is therefore respectfully requested to withdraw this corresponding objection.

Claim Rejections-35 U.S.C. 102

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Hikida et al. reference (U.S. Patent No. 5,620,914). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a semiconductor substrate, a silicon oxide layer, a gate electrode, and a side wall structure "which includes nitrogen formed over a second portion of said silicon oxide layer and adjacent said gate electrode". As further featured, "a thickness of said second portion of said

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silicon oxide layer is greater than a thickness of said first portion of said silicon oxide layer". Applicants respectfully submit that the Hikida et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that the Hikida et al. reference discloses all the features of claim 1 in Figs. 1(a)-1(f). The Examiner has interpreted side-wall structure 10 as particularly illustrated in Fig. 1(f) as the side wall structure of claim 1. However, sidewall spacer 10 is described in column 6, lines 54-57 of the Hikida et al. reference as a second conductive layer made of WSi (tungsten silicide). The Hikida et al. reference does not disclose a side wall structure including nitrogen, as in claim 1. The Hikida et al. reference therefore does not prevent diffusion of nitrogen into the silicon substrate of the structure, and thus is not directed to preventing hot-carrier degradation. Accordingly, Applicants respectfully submit that the semiconductor device of claim 1 distinguishes over the Hikida et al. reference as relied upon by the Examiner, and that this rejection of claims 1-3 is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 4-14, 16 and 17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Hikida et al. reference. This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 4 includes in combination a side wall structure "which includes nitrogen formed adjacent said gate electrode". As further

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featured, "said diffusion deterrent layer prevents nitrogen in said side wall structure from diffusing into said semiconductor substrate". As noted above, the Hikida et al. reference includes a side wall structure formed of conductive tungsten silicide. The Hikida et al. reference does not include a side wall structure including nitrogen, and therefore does not include a diffusion deterrent layer that prevents nitrogen in a side wall structure from diffusing into a semiconductor structure. Applicants therefore respectfully submit that the semiconductor device of claim 4 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection of claim 4 is improper for at least these reasons.

The method for manufacturing a semiconductor device of claim 5 includes in combination forming a side wall structure including nitrogen. As noted above, the Hikida et al. reference discloses a side wall structure formed of conductive tungsten silicide, not as including nitrogen. Accordingly, Applicants respectfully submit that the method for manufacturing a semiconductor device of claim 5 would not have been obvious in view of prior art as relied upon by the Examiner, and that this rejection of claims 5-13 is improper for at least these reasons.

The method for manufacturing a semiconductor device of claim 16 includes in combination forming a side wall structure including nitrogen, wherein the side wall structure is formed by CVD at a temperature exceeding 850°C. As noted above, the Hikida et al. reference does not disclose a side wall structure including nitrogen. More particularly, the Hikida et al. reference does not disclose forming a side wall structure including nitrogen by CVD at a temperature exceeding 850°C. Applicants therefore

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respectfully submit that the method for manufacturing a semiconductor device of claim 16 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection of claim 16 is improper for at least these reasons.

The method for manufacturing a semiconductor device of claim 17 includes in combination "forming a first portion of a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode" and "forming a second portion of said side wall structure on said first portion of said side wall structure over said second portion of said gate oxide layer and adjacent said gate electrode". As further featured, "said first portion of said side wall structure is formed by CVD at a temperature exceeding 850°C".

Applicants respectfully submit that conductive tungsten silicide side wall structure 10 in Fig. 1(f) of the Hikida et al. reference is not specifically described as being formed of a first portion and a second portion, as particularly featured in claim 17. Moreover, the Hikida et al. reference does not disclose or even remotely suggest that a first portion of a side wall structure is formed by CVD at a temperature exceeding 850°C. Accordingly, Applicants respectfully submit that the method for manufacturing a semiconductor device of claim 17 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection of claim 17 is improper for at least these reasons.

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Allowable Subject Matter

Applicants respectfully note the Examiner's acknowledgment that claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Although Applicants do not necessarily concede that the rejection of claim 14 is proper, claim 14 has been amended to include the features of claim 15 merely to expedite prosecution of this application. Clam 15 has been canceled. The Examiner is respectfully requested to acknowledge that claim 14 is allowed.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of two (2) months to June 14, 2002, for the period in which to file a response to the outstanding Office Action. The required fee is to be charged to our Deposit Account No. 50-0238.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Enclosures: Version with marked-up changes

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VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Specification:

Page 1, lines 10-12:

This is a counterpart of, and claims priority to, Japanese Patent Application No. 2000-[1250] 010250, filed on Jan. 17, 2000, the contents of which are incorporated herein by reference.

Page 9, lines 21-25:

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 222 are formed as seen in fig. 6(c). (Step 55) Subsequent steps are the same as those in the first embodiment. ([Step] Steps 56-58)

Page 10, lines 26-29:

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 322 are formed as seen in Fig. 9(b). (Step 84)

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Page 14, lines 1-7:

A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. The formation of the SiN sidewall layer is performed at a temperature of over 850°C [Experiments os]. In experiments, the [inventor] inventors have [shwon] shown that high temperature formation of the SiN sidewall reduces the hydrogen that diffuses into the semiconductor substrate. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 522 are formed. (Fig. 15(b), Step S144)

Page 17, lines 17-21:

The gate electrode material 716 and the cap layer material 720 are formed on the gate oxide layer 724. A lithography method and an anisotropic etching technique, such as a RIE method, are employed to etch the gate electrode material [616] 716 and the cap layer material 720. The gate electrode [616] 716 and the cap layer are thereby formed. (Step S202)

Additions/Deletions to the Claims:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a silicon oxide layer formed over a surface of said semiconductor substrate;

a gate electrode formed over a first portion of said silicon oxide layer; and

a side wall structure which includes nitrogen formed over a second portion of

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said silicon oxide layer and adjacent said gate electrode,

wherein a thickness of said second portion of said silicon oxide layer is greater than a thickness of said first portion of said silicon oxide layer.

2. (Amended) A semiconductor device as claimed in [claim. 1] claim 1, wherein the thickness of said second portion of said silicon oxide layer is at least twice the thickness of said first portion of said silicon oxide layer.

3. (Amended) A semiconductor device as claimed in [claim.1] claim 1, wherein the thickness of said second portion of said silicon oxide layer is at least 50% greater than the thickness of said first portion of said silicon oxide layer.

4. (Amended)[.] A semiconductor device comprising:

a semiconductor substrate;

a gate oxide layer formed over said semiconductor substrate;

a gate electrode formed over a first portion of said gate oxide layer;

a side wall structure which includes nitrogen formed adjacent said gate electrode; and

a diffusion deterrent layer formed between said side wall structure and said semiconductor substrate[;], wherein said diffusion deterrent layer prevents nitrogen in said side wall structure from diffusing into said semiconductor substrate,

wherein a thickness of said diffusion deterrent layer is greater than a thickness of

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said first portion of said gate oxide layer.

5. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode [and over] on a first portion of said gate oxide layer, said gate electrode having a cap layer formed thereon;

[forming a cap layer over said gate electrode;]

expanding a thickness of a second portion of said gate oxide layer other than said first portion of said gate oxide layer located under said gate electrode;

forming a side wall structure on [said] the expanded second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.

6. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.] claim 5, wherein the thickness of said second portion of said [silicon] gate oxide layer is at least twice [the] a thickness of said first portion of said [silicon] gate oxide layer.

7. (Amended) A method for manufacturing a semiconductor device as claimed

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in [claim.] claim 5, wherein the thickness of said second portion of said [silicon] gate oxide layer is at least 50% greater than [the] a thickness of said first portion of said [silicon] gate oxide layer.

8. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.] claim 5, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

9. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.] claim 6, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

10. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.] claim 7, wherein the thickness of said second portion of said gate oxide layer is expanded using CVD.

11. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.5] claim 5, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

12. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.6] claim 6, wherein the thickness of said second portion of said gate oxide

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layer is expanded using thermal oxidation.

13. (Amended) A method for manufacturing a semiconductor device as claimed in [claim.7] claim 7, wherein the thickness of said second portion of said gate oxide layer is expanded using thermal oxidation.

14. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer, said gate electrode having a cap layer formed thereon;

[forming a cap layer over said gate electrode;]

forming a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

expanding [the] a thickness of said second portion of said gate oxide layer located under said side wall structure using thermal oxidation, after said forming a side wall structure;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process.

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16. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on [the] a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer, said gate oxide having a cap layer formed thereon;

[forming a cap layer over said gate electrode;]

forming a side wall structure on a second portion of said gate oxide layer and adjacent said gate electrode, said side wall structure including nitrogen;

forming an intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process[;],

wherein [the] said side wall structure is formed by CVD at [the] a temperature exceeding 850°C.

17. (Amended) A method for manufacturing a semiconductor device, comprising:

forming a gate oxide layer on [the] a surface of a semiconductor substrate;

forming a gate electrode over a first portion of said gate oxide layer;

forming a cap layer over said gate electrode;

forming a first portion of a side wall structure over a second portion of said gate oxide layer and adjacent said gate electrode;

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forming a second portion of <u>said</u> side wall structure <u>on said first portion of said side wall structure</u> over [a] <u>said</u> second portion of said gate oxide layer and adjacent said gate electrode;

forming <u>an</u> intermediate insulating layer over said cap layer and said side wall structure; and

forming a contact hole in said intermediate insulating layer using a Self Aligned Contact process[;]<u>,</u>

wherein said first portion of <u>said</u> side wall structure is formed by CVD at [the] <u>a</u> temperature exceeding 850°C<u>.</u>

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